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(54) **VERTICAL CHANNEL TRANSISTOR STRUCTURE AND MANUFACTURING METHOD THEREOF**

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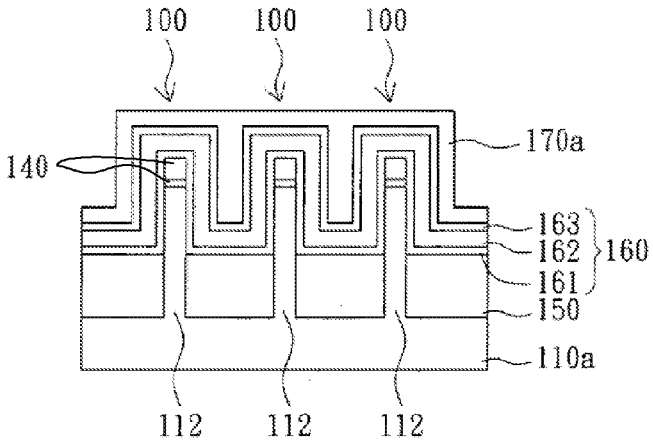
(57) **ABSTRACT**

A vertical channel transistor structure is provided. The structure includes a substrate, a channel, a cap layer, a charge trapping layer, a source and a drain. The channel is formed in a fin-shaped structure protruding from the substrate. The cap layer is deposited on the fin-shaped structure. The cap layer and the fin-shaped structure have substantially the same width. The charge trapping layer is deposited on the cap layer and on two vertical surfaces of the fin-shaped structure. The gate is deposited on the charge trapping layer and on two vertical surfaces of the fin-shaped structure. The source and the drain are respectively positioned on two sides of the fin-shaped structure and opposite the gate.

6 Claims, 12 Drawing Sheets



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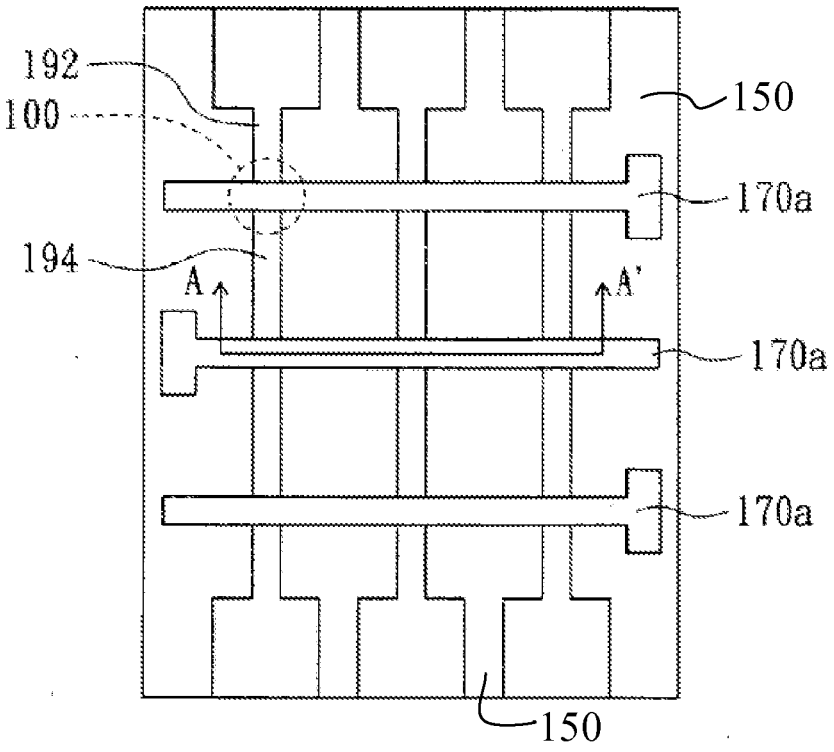
192
100
150
170a
194
A
A'
170a
170a
150

FIG. 1A

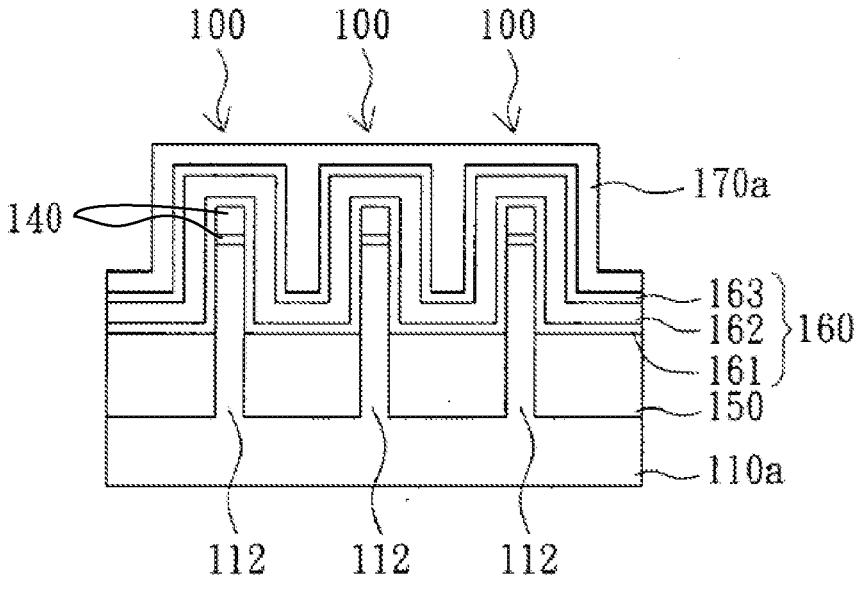
100
100
100
170a
140
163
162
160
161
150
110a
112
112
112

FIG. 1B

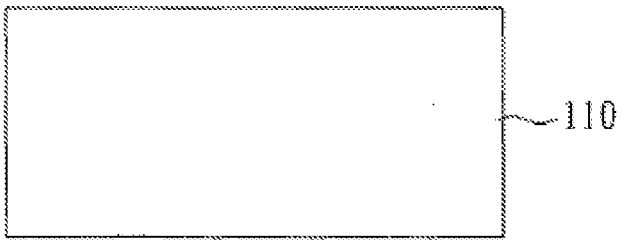

FIG. 2A

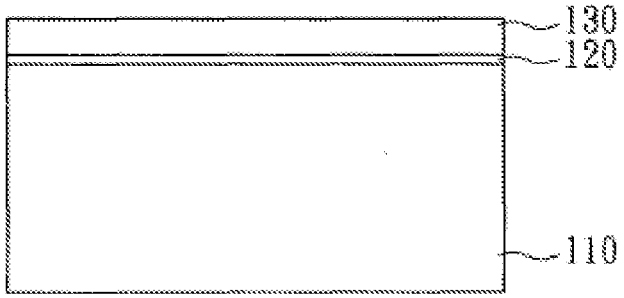

FIG. 2B

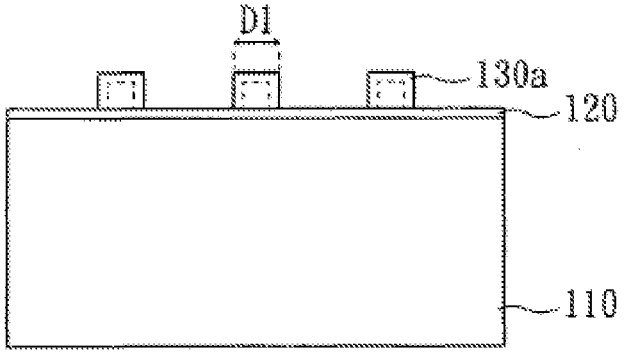

FIG. 2C

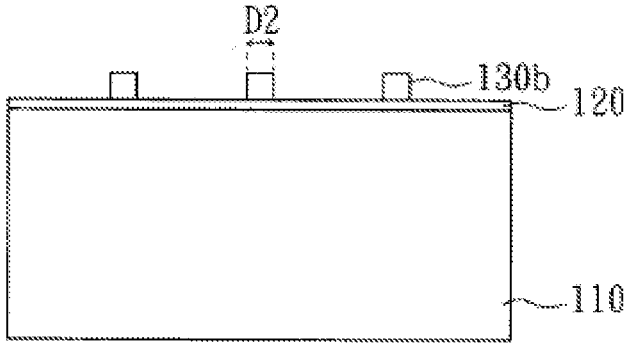

FIG. 2D

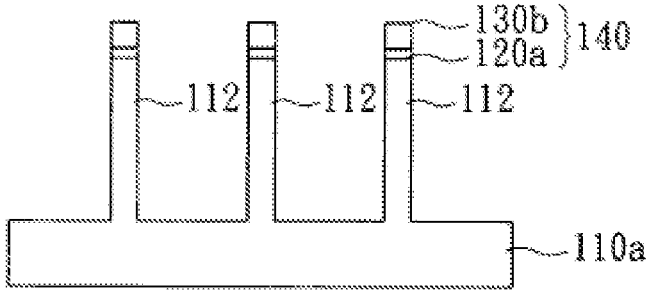

FIG. 2E

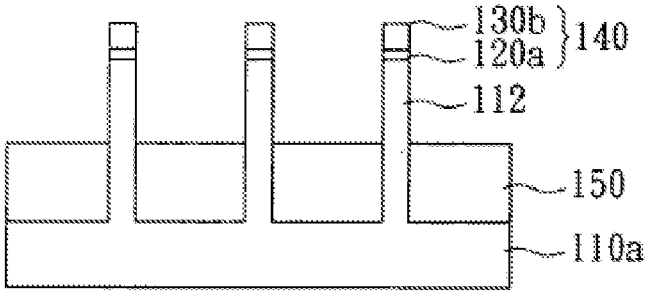

FIG. 2F

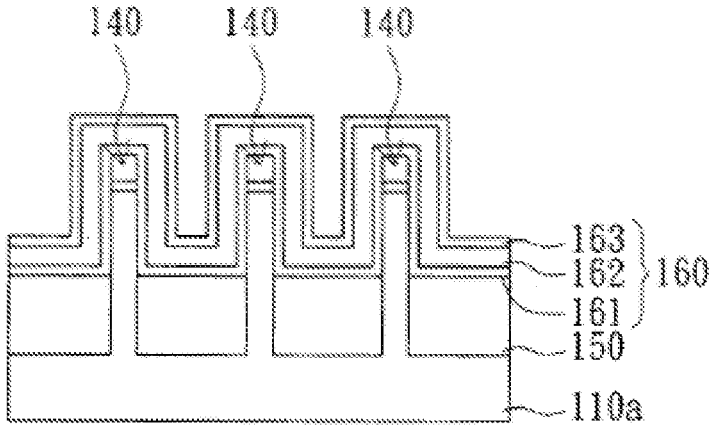

FIG. 2G

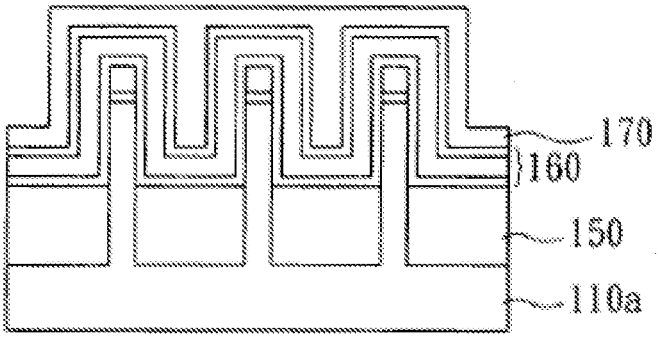

FIG. 2H

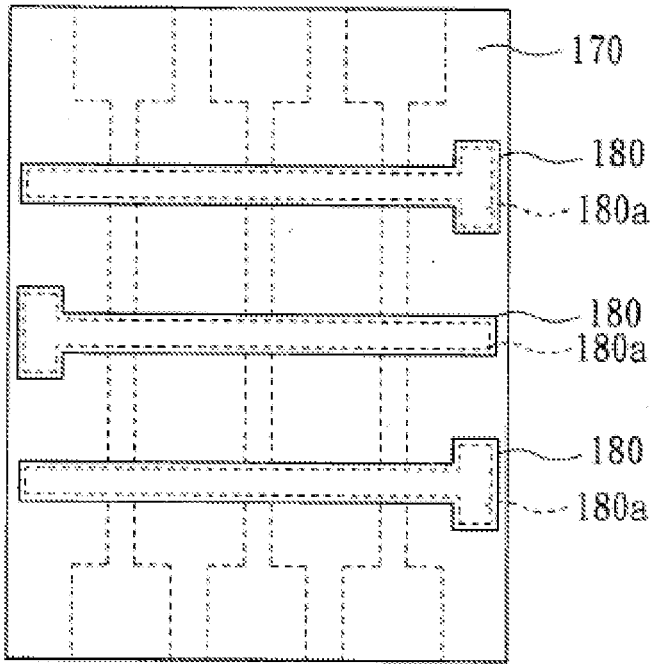

FIG. 2I

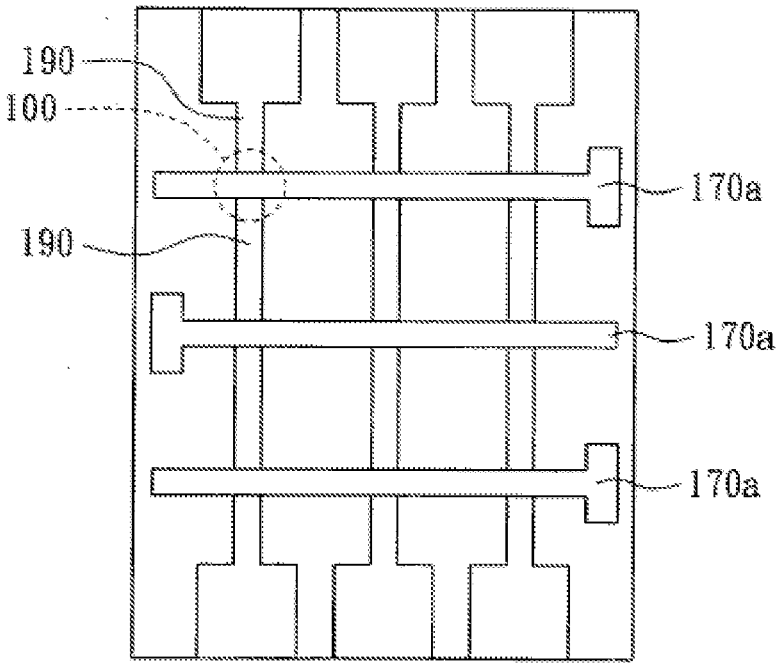

FIG. 2J

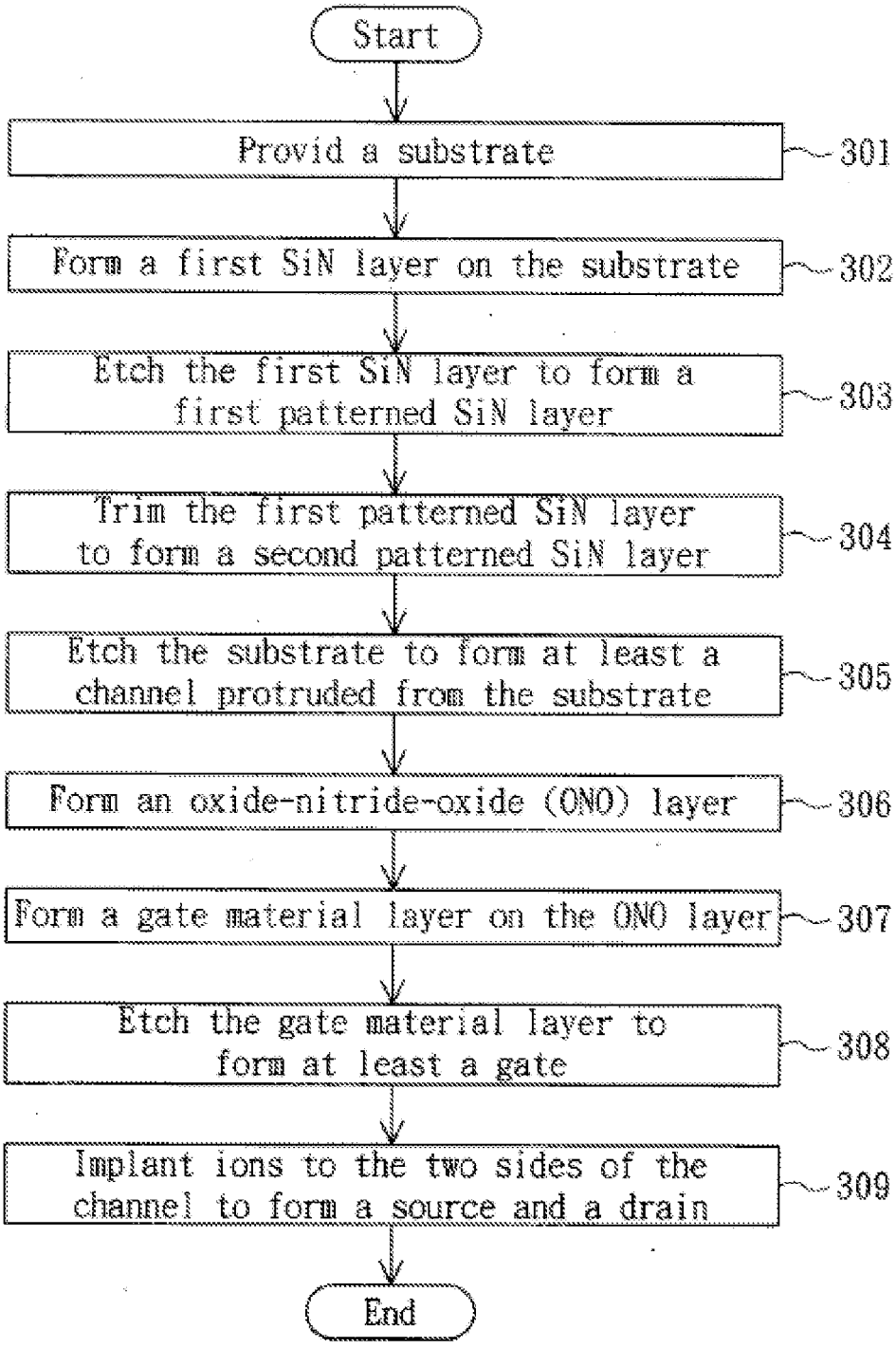
Start
Provid a substrate
301
Form a first SiN layer on the substrate
302
Etch the first SiN layer to form a first patterned SiN layer
303
Trim the first patterned SiN layer to form a second patterned SiN layer
304
Etch the substrate to form at least a channel protruded from the substrate
305
Form an oxide-nitride-oxide (ONO) layer
306
Form a gate material layer on the ONO layer
307
Etch the gate material layer to form at least a gate
308
Implant ions to the two sides of the channel to form a source and a drain
309
End

FIG. 3

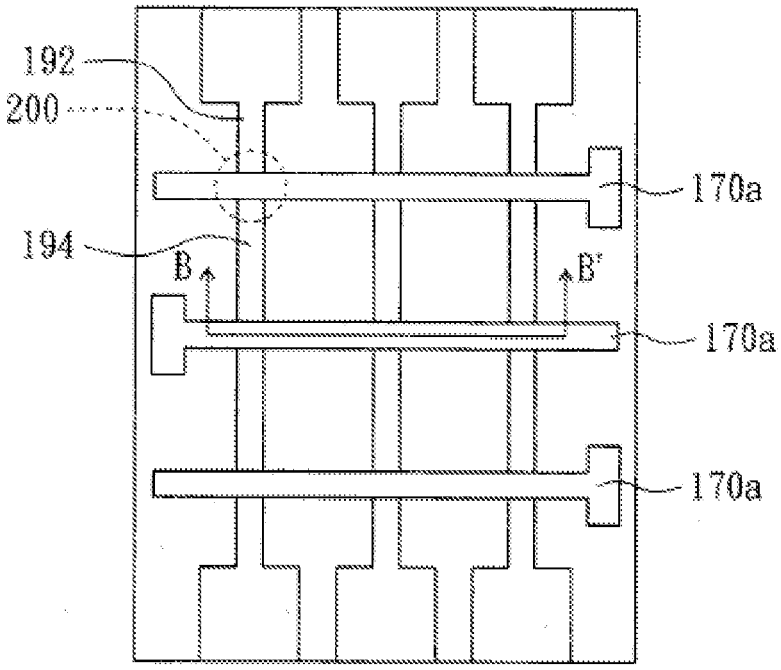
192
200
194
B
B'
170a
170a
170a

FIG. 4A

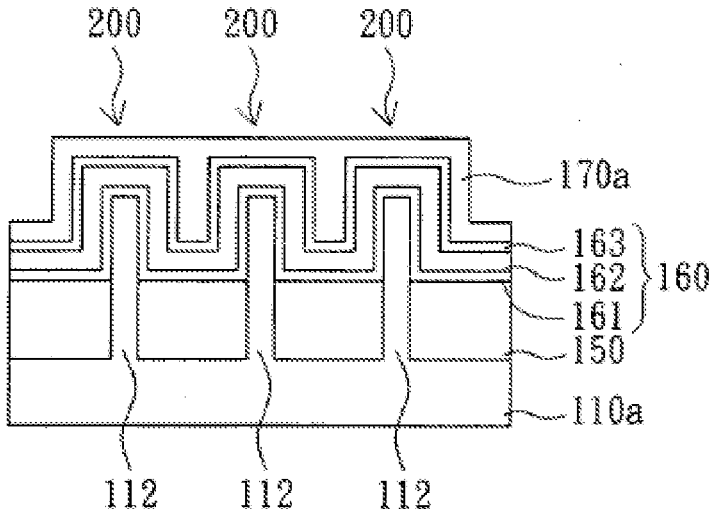
200
200
200
170a
163
162
161
160
150
110a
112
112
112

FIG. 4B

FIG. 5A

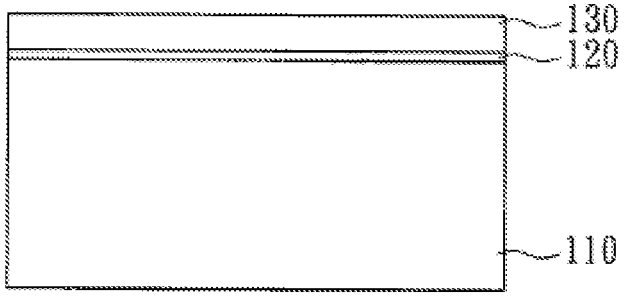

FIG. 5B

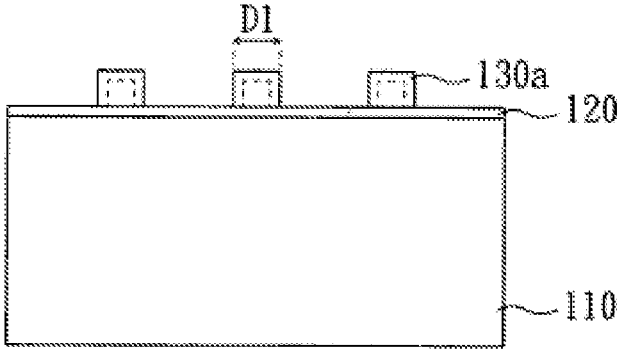

FIG. 5C

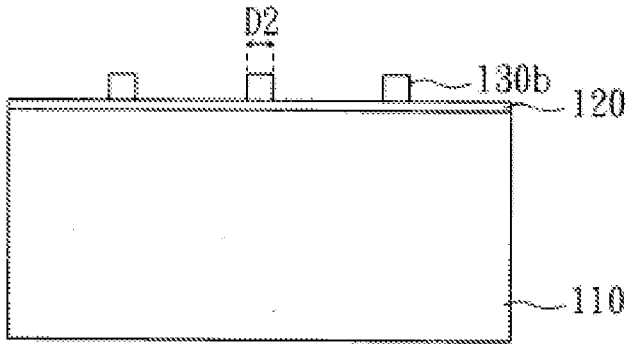

FIG. 5D

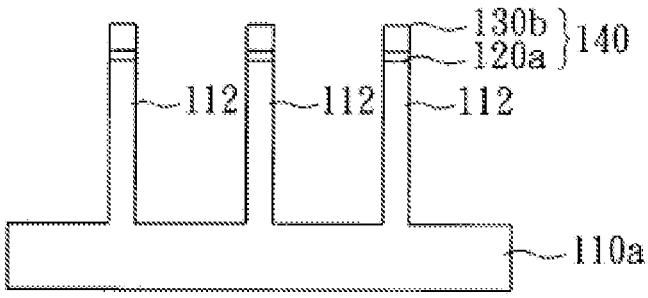

FIG. 5E

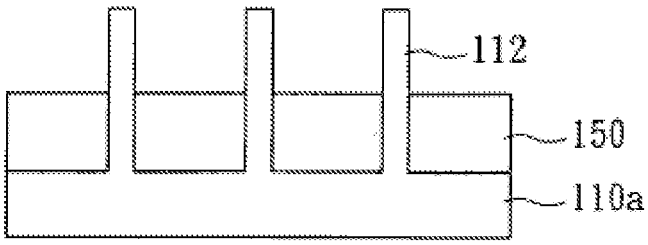

FIG. 5F

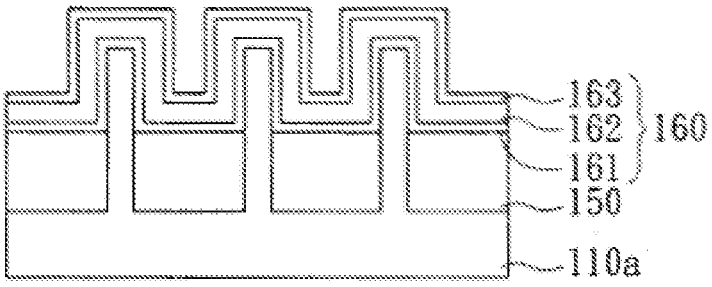

FIG. 5G

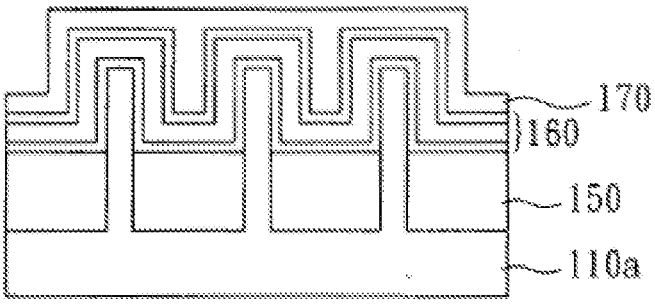

FIG. 5H

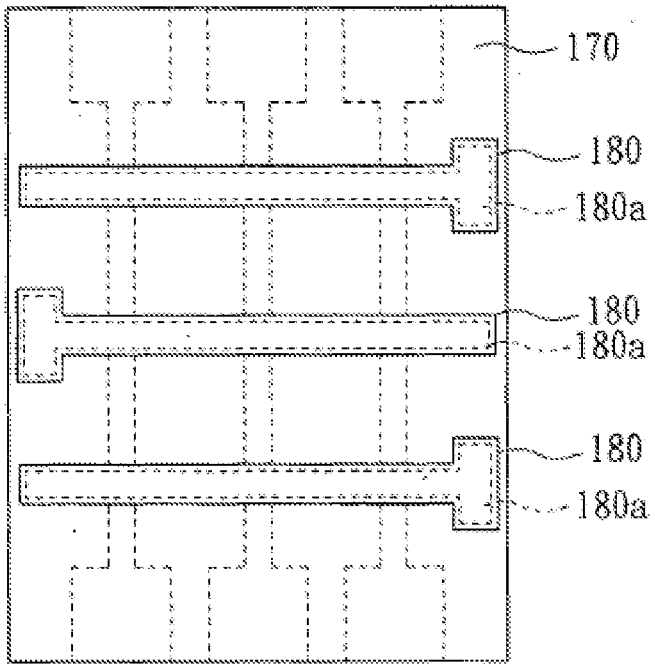

FIG. 5I

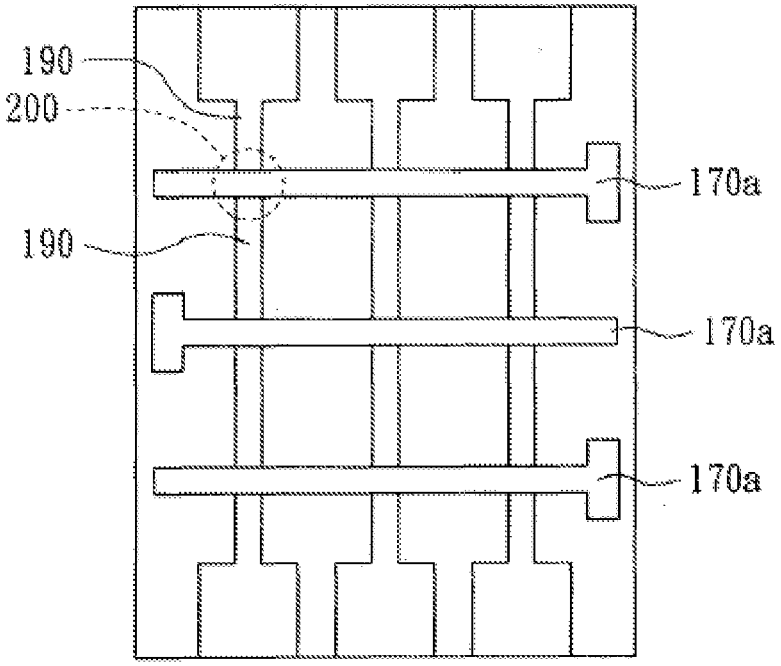

FIG. 5J

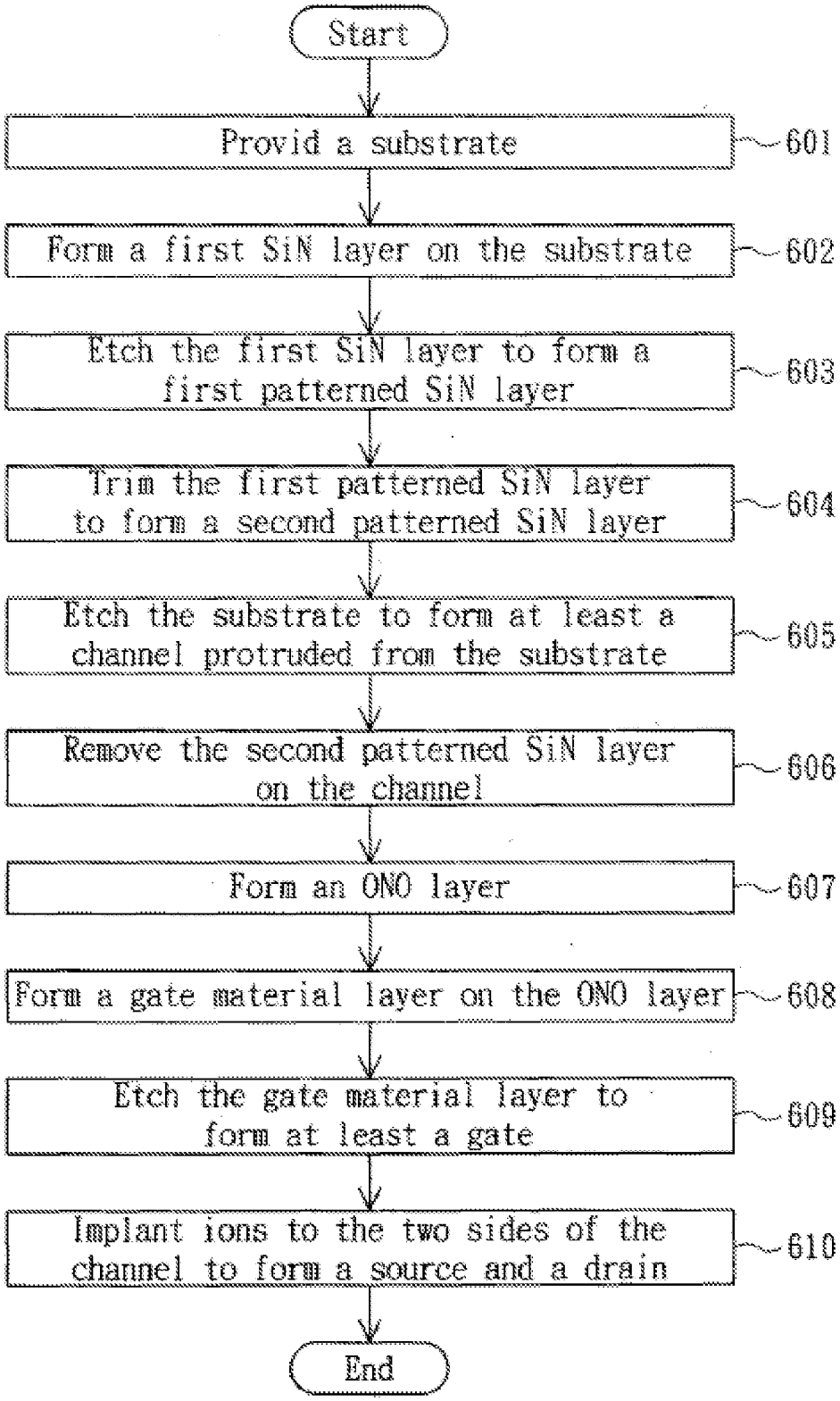
Start
Provid a substrate
601
Form a first SiN layer on the substrate
602
Etch the first SiN layer to form a first patterned SiN layer
603
Trim the first patterned SiN layer to form a second patterned SiN layer
604
Etch the substrate to form at least a channel protruded from the substrate
605
Remove the second patterned SiN layer on the channel
606
Form an ONO layer
607
Form a gate material layer on the ONO layer
608
Etch the gate material layer to form at least a gate
609
Implant ions to the two sides of the channel to form a source and a drain
610
End

FIG. 6

VERTICAL CHANNEL TRANSISTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

RELATED APPLICATIONS

This application is a divisional of U.S. patent application Ser. No. 11/545,575 filed on 11 Oct. 2006, now U.S. Pat. No. 7,811,890, which application is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates in general to a vertical channel transistor structure and a manufacturing method thereof, and more particularly to a vertical channel transistor structure with narrow channel and a manufacturing method therefor.

2. Description of the Related Art

Along with other advances in semiconductor manufacturing technology, the resolution of current semiconductor elements has reached the nanometer level. For example, the reduction in gate length and element pitch in memory units is carried on continually. Although the technology of photolithography has improved greatly, currently manufactured planar transistor structures have reached the limit of resolution, and the transistor elements manufactured thereby are apt to have the problems of electrostatic discharge (ESD), leakage, and decrease in electron mobility, resulting in short channel effect and drain induced barrier lowering (DIBL) effect. Thus, the double-gate or tri-gate vertical channel transistors capable of providing higher packing density, better carrier transport and device scalability, such as the fin field effect transistor (fin FET) for instance, have become transistor structures with great potential.

The fin FET transistor has a vertical channel that can be formed on the two lateral surfaces of the fin FET transistor and turns on the current by the double-gate or the tri-gate, hence having higher efficiency than conventional planar channel transistors.

When manufacturing a fin FET element with high resolution, expensive processes such as the photolithography process and the E-beam process are required. Therefore, the throughput can hardly be increased and large-scale production is difficult to achieve. There is another manufacturing method which reduces the channel width by applying oxidation to the etched channel. However, the element formed according to the above method has poor uniformity and unstable quality.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a vertical channel transistor structure and manufacturing method thereof. The fin-shaped structure whose width ranges between 10 nm~60 nm can be formed without changing the pitch of the element formed by way of exposing, such that the driving current for writing/reading data is effectively increased without incurring short channel effect or DIBL effect. The fin FET transistor formed according to the invention is small-sized, so the memory density can be improved significantly.

The invention achieves the above-identified object by providing a vertical channel transistor structure. The structure includes a substrate, a channel, a cap layer, a charge trapping layer, a source and a drain. The channel of the transistor structure is formed on a semiconductor body which protrudes from the substrate in a fin-shaped structure. The cap layer is deposited on the top of the fin-shaped structure. The cap layer and the fin-shaped structure have substantially the same width. The charge trapping layer is deposited on the cap layer and on two vertical surfaces of the fin-shaped structure. The gate straddles on the charge trapping layer and is positioned on the two vertical surfaces of the fin-shaped structure. The source and the drain are respectively positioned on two sides of the gate in the fin-shaped structure.

The invention further achieves the above-identified object by providing a manufacturing method of a vertical channel transistor structure. First, a substrate is provided. Next, a first SiN layer is formed on the substrate. Then, the SiN layer is etched to form a first patterned SiN layer. Next, the first patterned SiN layer is trimmed to form a second patterned SiN layer. Then, the substrate is etched to form at least a fin-shaped structure protruding from the substrate. Afterwards, a silicon oxide (SiO) layer is formed on top surface of the substrate. Next, an oxide-nitride-oxide (ONO) layer is formed on two vertical surfaces of the fin-shaped structure. Then, a gate material layer is formed on the ONO layer. Next, the gate material layer is etched to form at least a gate positioned on two lateral surfaces of the fin-shaped structure so that a straddle gate is formed over a vertical surface of the fin-shaped structure. Then, ions are implanted to two sides of the gate to form a source and a drain on the fin-shaped structure.

Other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A is a top view of a vertical channel transistor structure according to a first embodiment of the invention;

FIG. **1**B is a cross-sectional view along a cross-sectional line AA' of FIG. **1**A;

FIGS. **2**A~**2**J are manufacturing procedures of the vertical channel transistor structure according to the first embodiment;

FIG. **3** is a step flowchart of manufacturing the vertical channel transistor structure according to the first embodiment;

FIG. **4**A is a top view of the vertical channel transistor structure according to a second embodiment of the invention;

FIG. **4**B is a cross-sectional view along a cross-sectional line BB' of FIG. **4**A;

FIG. **5**A~**5**J are manufacturing procedures of the vertical channel transistor structure according to the second embodiment; and

FIG. **6** is a step flowchart of manufacturing the vertical channel transistor structure according to the second embodiment.

DETAILED DESCRIPTION OF THE INVENTION

First Embodiment

FIG. **1**A is a top view of a vertical channel transistor structure according to a first embodiment of the invention. FIG. **1**B is a cross-sectional view along a cross-sectional line AA' of FIG. **1**A. As shown in FIG. **1**B, the vertical channel transistor structure **100** includes a substrate **110***a*, a fin-shaped structure **112** protruding from the substrate **110***a* and a cap layer **140** deposited on the top of the fin-shaped structure **112**. The cap layer **140** and the fin-shaped structure **112** have substantially

the same width. In the present embodiment of the invention, the cap layer **140**, an intermediate product during the manufacturing process, includes a silicon dioxide (SiO_2) layer and a silicon nitride (SiN) layer. The SiN layer is positioned on the SiO_2 layer. A charge trapping layer **162** is deposited on the cap layer **140** and straddles the fin-shaped structure **112**. The charge trapping layer **162** is contained between a first SiO layer **161** and a second SiO layer **163**. The first SiO layer **161** is positioned between the charge trapping layer **162** and the fin-shaped structure **112**. The second SiO layer **163** is positioned between the charge trapping layer **162** and the gate **170***a*. The charge trapping layer **162** is made from SiN, aluminum oxide (Al_2O_3) or other material with high dielectric constant. In the present embodiment of the invention, the charge trapping layer **162** is made from SiN. The charge trapping layer **162**, the first SiO layer **161** and the second SiO layer **163** together form an oxide-nitride-oxide (ONO) layer as a storage structure, such that the vertical channel transistor structure **100** has data-writing/data-erasing function. The gate straddles the charge trapping layer **162** and two vertical surfaces on the fin-shaped structure **112**. The gate **170***a* can turn on the circuit on the two vertical surfaces of the fin-shaped structure **112**, and the structure formed thereby is called the double-gate structure. The gate **170***a* can be made from N+ polysilicon, P+ polysilicon, or metal. As shown in FIG. **1**A, the source **192** and the drain **194** are respectively positioned on the two sides of the gate **170***a*. The present embodiment of the invention is a NAND gate structure, so the source and the drain can be exchanged, and the source or the drain between any two vertical channel transistor structures **100** is not only a source for one transistor but also a drain for another. The line width of the fin-shaped structure **112** approximately ranges between 10 nm~60 nm.

As shown in FIG. **1**B, the vertical channel transistor structure **100** further includes a thick SiO layer **150** positioned on the substrate **110***a*. The purpose of the thick SiO layer **150** is to prevent substrate being turned on to cause leakage.

The application of the present embodiment of the invention is exemplified below by the manufacturing process of a NAND memory. Referring to FIGS. **2**A-**2**J, manufacturing procedures of the vertical channel transistor structure according to the first embodiment are shown. Also referring to FIG. **3**, a step flowchart of manufacturing the vertical channel transistor structure according to the first embodiment is shown.

First, referring to FIG. **2**A, at step **301** a substrate **110** is provided. The substrate **110** can be a bulk silicon substrate or a silicon-on-insulator (SOI) substrate.

Next, referring to FIG. **2**B, a first SiN layer **130** is formed on the substrate **110** as indicated in step **302**. In the present embodiment of the invention, a pad SiO layer **120** is preferably formed between the substrate **110** and the first SiN layer **130**. The present embodiment of the invention forms a transistor structure with N-type channel. Therefore, in the present step, P-type ions are implanted to the substrate **100** for enabling the substrate **100** to have better function in subsequent processing of forming the channel. However, the present embodiment of the invention is not limited thereto. If a transistor having P-type channel is to be formed, then N-type ions are implanted to the substrate **100**.

Then, referring to FIG. **2**C, the first SiN layer **130** is etched to form a first patterned SiN layer **130***a* as indicated in step **303**. Step **303** includes the sub-steps of forming a first patterned photoresist layer (not illustrated) on the first SiN layer **130**; etching the first SiN layer **130** to form the first patterned SiN layer **130***a*; and removing the first patterned photoresist layer. The first patterned SiN layer **130***a* has a pattern with line width D**1**. The present step can be performed using a reactive ion etching (RIE) method.

Next, referring to FIG. **2**D, the first patterned SiN layer **130***a* is trimmed to form a second patterned SiN layer **130***b* as indicated in step **304**. After the trimming process, the second patterned SiN layer **130***b* has a pattern with line width D**2**. The line width D**2** approximately ranges between 10 nm~60 nm. Since the hot-phosphoric-acid (HDP) possesses excellent etching selectivity towards SiN and SiO, that is used to trim the first patterned SiN layer **130***a* in the present step.

Referring to FIG. **2**E, the substrate **110** is etched to form a substrate **110***a* first and form a fin-shaped structure **112** protruding from the substrate **110***a* as indicated in step **305**. In the present embodiment of the invention, the pad SiO layer **120** is preferably etched to form a pad SiO layer **120***a* according to RIE method first, and then the substrate **110** is etched to form a fin-shaped structure **112** next. The pad SiO layer **120***a* and the second patterned SiN layer **130***b* together form the cap layer **140**.

Next, referring to FIG. **2**F, a thick SiO layer **150** contacting two lateral surfaces of the fin-shaped structure **112** is formed. In the present step, the thick SiO layer **150** is deposited by high density plasma (HDP) deposition. The thick SiO layer **150** restricts the height of a channel on the fin-shaped structure **112**, such that the current can only flow through the part of the fin-shaped structure **112** above the thick SiO layer **150**.

Then, referring to FIG. **2**G, an oxide-nitride-oxide (ONO) layer **160** is formed as indicated in step **306**. The ONO layer **160** is deposited on the cap layer **140**, the two vertical surfaces of fin-shaped structure **112** and thick SiO layer **150**. The ONO layer includes a first SiO layer **161**, a charge trapping layer **162** and a second SiO layer **163**. In the present embodiment of the invention, the charge trapping layer **162** is made from SiN, and can be replaced by aluminum oxide (Al_2O_3) or other high dielectric constant material.

Next, referring to FIG. **2**H, a gate material layer **170** is formed on the ONO layer **160** as indicated in step **307**.

Then, referring to FIG. **2**I, the gate material layer **170** is etched to form at least a gate straddling the fin-shaped structure **112** as indicated in step **308**. Preferably, the following steps are performed before step **308**. First, a second SiN layer (not illustrated) is formed on the gate material layer **170**. Next, a second patterned photoresist layer (not illustrated) is formed on the second SiN layer. Then, the second SiN layer is etched to form a third patterned SiN layer **180**. Next, the second patterned photoresist layer is removed. Then, the third patterned SiN layer **180** is trimmed to form a fourth patterned SiN layer **180***a*. Then, referring to FIG. **2**J, the gate material layer **170** is etched to form a gate **170***a* according to the pattern of the fourth patterned SiN layer **180***a*. After the gate **170***a* is formed, the step of removing the fourth patterned SiN layer **180***a* is preferably further included. Thus, a gate structure whose line width approximately ranges between 10 nm~60 nm is formed.

Next, ions are implanted in the fin-shaped structure **112** to the two sides of the gate **170***a* to form a source/drain **190** as indicated in step **309**. Thus, the main structure of the NAND gate memory of the vertical channel transistor structure **100** is formed. The present embodiment of the invention is exemplified by the formation of an N-type channel transistor, so N-type dopants are used in the present step. However, if a P-type channel transistor is to be formed, then P-type dopants are used in the present step.

Second Embodiment

Referring to FIG. **4**A and FIG. **4**B. FIG. **4**A is a top view of the vertical channel transistor structure according to a second embodiment of the invention. FIG. **4**B is a cross-sectional

view along a cross-sectional line BB' of FIG. **4**A. The vertical channel transistor structure **200** of the present embodiment differs with the vertical channel transistor structure **100** of first embodiment in that the cap layer **140** is removed. As for other elements, the vertical channel transistor structure **200** and the vertical channel transistor structure **100** are substantially the same, so the same reference numbers are used and their functions are not repeated here.

As the oxide layer **140** is removed, the gate **170***a* can turn on the circuit on the top surface of the fin-shaped structure **112**, and the structure formed thereby is called the tri-gate structure.

The application of the present embodiment of the invention is again exemplified by the manufacturing process of a NAND gate memory array structure (NAND memory). Referring to FIGS. **5**A-**5**J, manufacturing procedures of the vertical channel transistor structure according to the second embodiment are shown. Also referring to FIG. **6**, a step flowchart of manufacturing the vertical channel transistor structure according to the second embodiment is shown.

First, referring to FIG. **5**A, a substrate **110** is provided as indicated in step **601**.

Next, referring to FIG. **5**B, a first SiN layer **130** is formed on the substrate **110** as indicated in step **602**. In the present embodiment of the invention, a pad SiO layer **120** is preferably formed between the substrate **110** and the first SiN layer **130**. Furthermore, in the present step, P-type ions are implanted to the substrate **110** for enabling the substrate **110** to have better function in subsequent processing of forming the channel. However, the present embodiment of the invention is not limited thereto. If a transistor with P-type channel is to be formed, then N-type ions are implanted to the substrate **110**.

Then, referring to FIG. **5**C, the first SiN layer **130** is etched to form a first patterned SiN layer **130***a* as indicated in step **603**. Step **603** includes the following steps of forming a first patterned photoresist layer (not illustrated) on the first SiN layer **130**; etching the first SiN layer **130** to form a first patterned SiN layer **130***a*; and removing the first patterned photoresist layer. The first patterned SiN layer **130***a* has a pattern with line width D**1**.

Next, referring to FIG. **5**D, the first patterned SiN layer **130***a* is trimmed to form a second patterned SiN layer **130***b* as indicated in step **604**. The second patterned SiN layer **130***b* has a pattern with line width D**2**. The line width D**2** approximately ranges between 10 nm~60 nm.

Then, referring to FIG. **5**E, the substrate **110** is etched to form a substrate **110***a* and form a fin-shaped structure **112** protruding from the substrate **110***a* as indicated in step **605**. In the present embodiment of the invention, the pad SiO layer **120** is preferably etched to form a pad SiO layer **120***a* according to RIE method first, then the substrate **110** is etched to form a fin-shaped structure **112** next. Meanwhile, the pad SiO layer **120***a* and the second patterned SiN layer **130***b* together form the cap layer **140**.

Next, referring to FIG. **5**F, a thick SiO layer **150** preventing lower portions of the vertical surfaces of the fin-shaped structure **112** being turned on is formed. Meanwhile, like step **606**, the second patterned SiN layer **130***b* on the fin-shaped structure **112** is removed by hot-phosphoric-acid (H_3PO_4), and the pad SiO layer **120***a* is preferably removed by hydrofluoric acid (HF). The step of removing the second patterned SiN layer **130***b* and the pad SiO layer **120***a* can be performed before or after the step of forming the thick SiO layer **150**.

Then, referring to FIG. **5**G, an oxide-nitride-oxide (ONO) layer **160** is formed as indicated in step **607**. The ONO layer **160** is deposited on the top surface, side wall vertical surfaces of fin-shaped structure **112** and on the thick SIO layer **150**. The ONO layer **160** includes a first. SiO layer **161**, a charge trapping layer **162** and a second SiO layer **163**. In the present embodiment of the invention, the charge trapping layer **162** can be made from SiN or aluminum oxide (Al_2O_3) or other high dielectrical constant material.

Next, referring to FIG. **5**H, a gate material layer **170** is formed on the ONO layer **160** as indicated in step **608**.

Then, referring to FIG. **5**I, the gate material layer **170** is etched to form at least a gate positioned on the top surface of fin-shaped structure **112** and the vertical surfaces of the fin-shaped structure **112** as indicated in step **609**. Preferably, the following steps are performed before step **609**. First, a second SiN layer (not illustrated) is formed on the gate material layer **170**. Next, a second patterned photoresist layer (not illustrated) is formed on the second SiN layer. Then, the second SiN layer is etched to form a third patterned SiN layer **180**. Next, the second patterned photoresist layer is removed. Then, the third patterned SiN layer **180** is trimmed to form a fourth patterned SiN layer **180***a*. Then, referring to FIG. **2**J, the gate material layer **170** is etched to form the gate **170***a* according to the pattern of the fourth patterned SiN layer **180***a*. After the gate **170***a* is formed, the step of removing the fourth patterned SiN layer **180***a* is preferably further included.

Next, proceeding to step **610**, ions are implanted on the fin-shaped structure **112** on the two opposing sides of the gate **170***a* to form a source/drain **190**. Thus, the main structure of the vertical channel transistor structure **200** of the NAND memory is formed.

According to the vertical channel transistor structure and manufacturing method thereof disclosed in the above embodiments of the invention, the line width of the pattern formed by SiN is further reduced by hot-phosphoric-acid, and the vertical channel transistor structure whose fin-shaped structure width ranges between 10 nm~60 nm is manufactured without changing the current exposing apparatus, that is, without changing the pitch of the element formed by way of exposing. The invention effectively increases the driving current for writing/reading data without increasing short channel effect or DIBL effect. The fin FET transistor formed according to the invention is small-sized, so the memory density is improved significantly. A transistor with a narrow fin-shaped structure can be manufactured according to the technology of the invention in large scale production and at low cost without employing expensive exposing apparatus. The invention adopts SiN as a hard mask and has better performance in resisting ion impact than a conventional photoresist layer. Thus, uniform semiconductor elements can be formed by way of etching without increasing the thickness of photoresist layer according to the technology of the invention.

While the invention has been described by way of example and in terms of preferred embodiments, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

The invention claimed is:

1. A vertical channel transistor array, comprising:

a substrate;

a plurality of channels protruded from the substrate;

a plurality of cap layers on the plurality of channels, wherein cap layers in the plurality of cap layers and channels in the plurality of channels substantially have the same width, wherein the cap layers comprise a sili-

con nitride (SiN) layer positioned on a silicon dioxide (SiO2) layer, and the SiN layer has a top surface and two vertical surfaces;

a multilayer charge trapping layer directly on the top surface and the two vertical surfaces of the SiN layer of the plurality of cap layers and on two vertical surfaces of the channels in the plurality of channels, the multilayer charge trapping layer including at least a first oxide layer, a first charge trapping layer on the first oxide layer, and a second oxide layer on the first charge trapping layer;

a plurality of word lines, word lines in the plurality of word lines straddling on the multilayer charge trapping layer and positioned on the two vertical surfaces of the channels in the plurality of channels; and

sources and drains respectively positioned on the two vertical sides of the channels in the plurality of channels,

wherein a channel in the plurality of channels in between adjacent ones of the sources and the drains, and in between the substrate and a word line of the plurality of word lines, supports only one transistor,

wherein the array is arranged as a plurality of series-connected NAND strings having opposite ends that end in transistors, and every transistor in the plurality of series-connected NAND strings includes one of the cap layers in the plurality of cap layers that comprises the silicon dioxide (SiO2) layer and the silicon nitride (SiN) layer.

2. The vertical channel transistor array according to claim **1**, further comprising a thick silicon oxide (SiO) layer positioned on the substrate.

3. The vertical channel transistor array according to claim **1**, wherein the first charge trapping layer is made from SiN or aluminum oxide (Al_2O_3).

4. The vertical channel transistor array according to claim **1**, wherein the substrate is a bulk silicon substrate or a silicon-on-insulator (SOI) substrate.

5. The vertical channel transistor array according to claim **1**, wherein the gate is made from N+ polysilicon, P+ polysilicon, or metal.

6. The vertical channel transistor array according to claim **1**, wherein a line width of the channel approximately ranges between 10 nm~60 nm.

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